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Design SVM Classifier for Automatic Modulation Recognition Systems

Mohamed Elhady Keshk[*,†], Dagvasumberel Amartuvshin, Rafael Rodriguez, and Kenichi Asami

Department of Applied Science for Integrated System Engineering, Kyushu Institute of Technology,
1-1 Sensui-cho, Tobata-ku, Kitakyushu-shi, Fukuoka 804-8550, Japan

SUMMARY

Recently, Small satellites became the trend of most investment in space field. One of the problems that face the satellites missions that Ground Control Stations (GCSs) can communicate with limited number of satellites and vice versa based on the modulation techniques. To develop a universal GCS and/or satellite, it is required to use multiple receivers which increase both the complexity and cost. One of the solutions is to classify the modulation technique of the received signal and use the result to partially reconfigure FPGA with the suitable demodulator. In this paper, Xilinx Vivado® and Mathworks MATLAB® tools are used together to implement and test Support Vector Machine Classifier (SVMC) system on Xilinx Kintex®-7 kc7k160tfbg484-1 FPGA. To demonstrate SVMC system, Discrete Wavelet Transform (DWT) is used to extract the features of received modulated signal and depending on these features, SVM can classify the modulation technique. BPSK and QPSK modulation techniques are implemented and used as an evaluation to SVMC. MATLAB tool is used to reduce the complexity of the VHDL design and to test the system performance in the presence of Adaptive White Gaussian Noise (AWGN) with Signal to Noise Ratio (SNR) from -10 to 20 and the results show good performance of the system in low SNR

KEY WORDS: Support Vector Machine; Automatic Modulation Recognition; FPGA; Software Defined Radio; M-ary Phase Shift Keying

[*] Corresponding author. Mohamed Elhady Keshk.
[†] E-mail: mohaelha@es.ise.kyutech.ac.jp.
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NOMENCLATURE

b	=	SVM bias
$g(x)$	=	classification function
$K(X_i, X_j)$	=	kernel function
W	=	normal to hyperplane
X_i	=	support vectors
X_j	=	extracted features
σ	=	Sigma parameter of radial base function

1. INTRODUCTION

Most of Ground Control Stations (GCSs) communicate with limited number of satellites. One of the reasons can be described as not all the satellites use the same modulation techniques. Which means, to have a GCS capable of communicating with satellites of different modulation techniques, this GCS should have all the corresponding demodulators. i.e., GCS should have many transceivers which increase the complexity and the cost of that GCS. And to have a satellite that can communicate with different GCSs (especially for satellite cooperation projects), so this satellite should have many transceivers inside and this is difficult and increases the complexity and cost of the satellite. One of the solutions is the implementation of a classifier for Automatic Modulation Recognition (AMR) of the received signal.

AMR is the classification of the received modulation signal. i.e., it has to identify the modulation scheme and type of received signal it is considered the intermediate stage between detection and demodulation stages of a communication system. AMR is the key role in the implementation of advanced wireless communication system especially for satellite communication system.

Two famous approaches are used to implement the classifier of received modulated signals; the Decision-Theoretic (DT) approach based on likelihood function, and the Pattern Recognition (PR) approach based on extracting unique measurable values (features) of the signal [1]. DT approach based on multiple hypothesis testing and has high performance in terms of correct classification percentage (optimal) but the drawbacks of this approach are high computational complexity which leads to that the classifier is impractical, and the sensitivity to impairments as frequency and phase offset. On the other hand, PR approach based on pattern matching and is suboptimal, simple to implement, and robust.

Classification system based on features that extracted from different modulations using Stockwell- transform and classified using different classification techniques such as Artificial Neural Network (ANN) and SVM has studied in [1]. AMR system is implemented using DWT to extract the transient characteristics of the modulation and based on a threshold value; and the modulation type is being recognized [2]. Two stages AMR system is implemented using energy detection (spectrum sensing) and modulation classification stages, and Principle Component Analysis (PCA) and ANN were used for the classification stage [3]. A classification system is implemented using predefined templates in Wavelet Domain (WD) stored in receiver side for several modulations which has been generated using DWT then matching these templates with the one initiated during real-time [4]. New technique using 8PSK demodulator output as features extraction and bayes classifier for classification [5]. Cumulants and ANN are used for features extraction and classification in AMR system [6]. Other studies using features extracted from FFT then compare them with some threshold values to make the decision [7], and using higher order cumulants as features and K- Nearest Neighbor as a classifier [8].

In this paper, SVM classifier (SVMC) in AMR system is described. SVMC is implemented using Vivado 2015.2, MATLAB r2015b, and applied on Kintex-7 FPGA kit. SVMC consists of two modules; features extraction (using DWT), and classification (using SVM) modules. DWT is used for extracting the features of M-ary Phase Shift Keying (MPSK) signal, and for classification, SVM is used as a binary classifier. MATLAB tool has an important role in the implementation of the design. MATLAB tool helps Vivado tool in implementing SVMC design with less resources and low power consumption. To evaluate the performance of SVMC, Modulation Signal Generator (MSG) is implemented to proof the concept and performance of SVMC it is required to generate two phase shift keying modulations, BPSK and QPSK which are used in satellite communication system. Then these modulation signals will act as the input to the classifier to test the classifier performance

This paper is organized as follows, section 2 introduces the principle of the SVMC system, section 3 describes VHDL based SVMC design, section 4 describes presents the simulations and results. Section 5, concludes the paper. Section 6, describes future work.

2. SVMC SYSTEM PRINCIPLE

SVMC consists of 3 stages of DWT and SVM modules. Received modulated signal is passed through 3 stages of DWT to extract the features of the modulations technique and these features will be classified by SVM module to generate the classification decision. Implementation of a SVM on FPGA increases the complexity of the design, so MATLAB tool will be used to reduce this complexity by implement training stage of SVM then providing VHDL design with necessary parameters to implement the classification function without the need to implement full SVM system (training and classification) on FPGA. According to the classification decision, the received modulated signal will be known. The dotted lines mean that operations are done offline. Fig.1 shows SVMC principle.

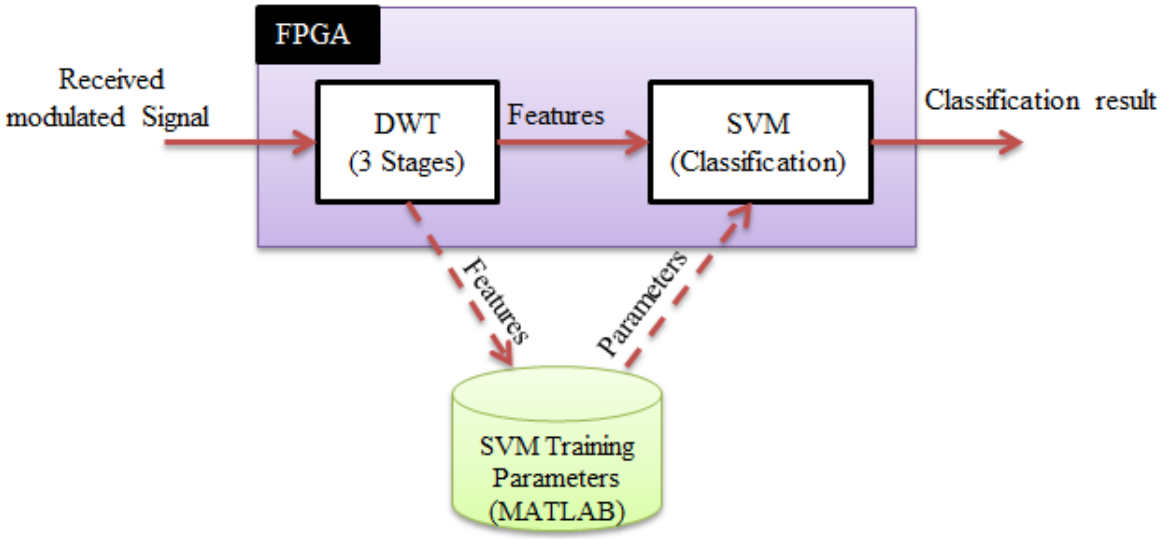

Figure 1 SVMC Principle

3. VHDL BASED SVMC DESIGN

SVMC module is implemented in the receiver module of a communication system. SVMC module consists of two modules; features extraction module and classification module. Where a received M-PSK signal is the input to DWT features extraction module and the output of this module feeds the input of the classifier to obtain the classification decision to know which M-PSK signal type is received.

3.1. DWT Module

Implementation of DWT module is required three stages of DWT to extract features of the BPSK and QPSK modulated signals. As the number of stages increases, less number of features represents the modulated signal as seen in Fig. 2 [2]. According to this paper purpose, it is not practical to implement the whole blocks in Fig. 2, just the colored path is required to obtain the DWT coefficients (features) as seen in Fig.2.

To implement DWT, three stages of Finite Impulse Response (FIR) IP core filter are used as seen in Fig. 3.Two LPF filters followed by one HPF with decimation of 2 are required to obtain the required level of DWT features. The implementation of complete DWT system is mandatory for reconstruction of images in imaging processing projects. Filter coefficients are obtained from MATLAB tool according to the type of the wavelet type. In this paper, daubechies wavelet type (db5) is used. After obtaining the coefficients from MATLAB tool, the filters become ready to extract the features.

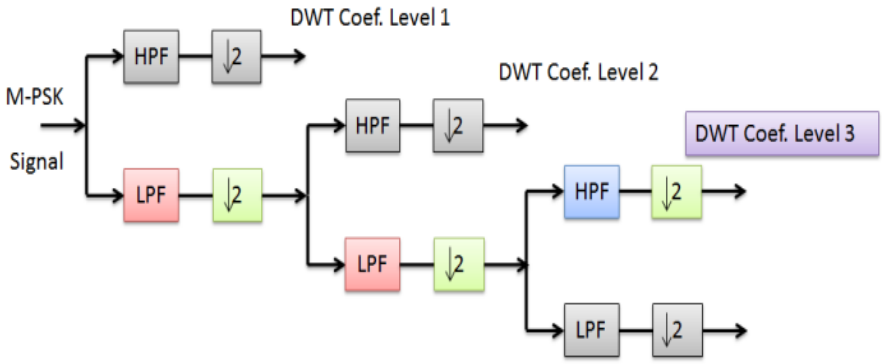

Figure 2 Three Stages of DWT

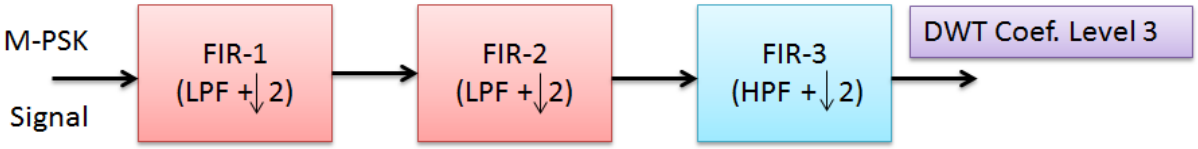

Figure 3 Implementation of DWT Stages using FIR

3.2. SVM Module

The extracted features from the previous stage are the input of SVM module. Implementation of the two stages of SVM (Training and classification stages) into Kintex-7 FPGA consumes a lot of resources and therefore increases the power consumption. So the efficient way to overcome this problem is to using MATLAB tool to train the classifier with the extracted features (offline training) then SVM parameters can be obtained from the training results of MATLAB tool to construct the classifier to classify the modulation in run time on FPGA using VHDL code.

SVM is one of the classifiers that used in classification process. The first objective of SVM is to maximize the margin between the closest data points of two different classes. The second objective is to be sure that all data points belong to their correct classes. SVM classifies the points from two linearly separable sets in two classes by solving a quadratic optimization problem in order to find the optimal separating hyper-plane between these two classes, Where it can classify data points from two linearly separable sets into their corresponding classes, also expanded to be used for the nonlinear cases by transforming the input data into a nonlinear space using Kernel functions [9]. Mapping function Φ (.) is considered dot product that transforms nonlinear classification problems from input space to linear features space (separable problem) where the classification can become easier as seen in Fig. 4 [10].

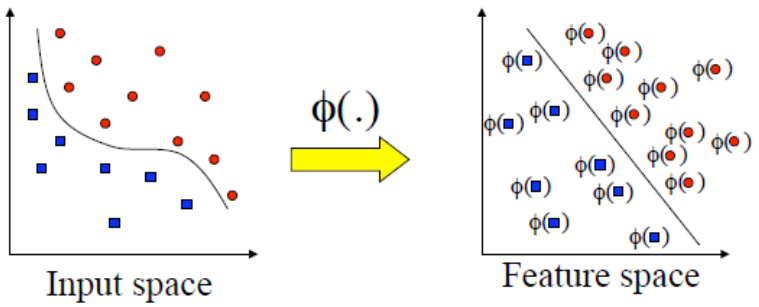

Figure 4 Kernel Function Transformations

SVM classification equation for nonlinear classification problems can be expressed mathematically as in Eq. 1 [9, 10].

$$g(X_j) = W.\ K(X_i , X_j) + b \quad (1)$$

Where $g(X_j)$ is the classification function, W (weight vector) is the normal to hyper plane, $K(X_i , X_j)$ is Kernel function, X_i is a support vectors vector, X_j is the data point (features) vector, b is the bias and it is a scaler quantity.

SVM module is used to classify the extracted features from received digital modulated signal into two classes; BPSK class and QPSK class. Before the classification, offline training process has to be implemented using MATLAB r2015b tool to train SVM on the extracted features from DWT to label these features with the correct class. The purpose of implementing this process in MATLAB is to obtain the required parameters for the classifier in SVM module which reduces the complexity of AMR system.

To classify BPSK and QPSK modulation it is required to select the proper kernel function that gives the best classification accuracy, many tests have done on the available kernel function with the extracted features, and the one with highest accuracy will be used.

Four different kernel functions have been selected and tested using MATLAB r2015b Tool using svmtrain and svmclassify functions. These kernel functions are Linear, Quadratic, Polynomial, and Radial Base Function (RBF) as shown in Table 1.

Selection of a kernel function depends on the accuracy of each one. RBF kernel function is selected to be the suitable kernel function because of its high classification accuracy with respect to the others kernel functions as described in section 5.

Table 1: Kernel Functions Equations

Kernel Function	Equation
Linear	Xi . Xj
Quadratic	((Xi . Xj) + 1)
Polynomial	$((Xi . Xj) + 1)^d$
Radial Base Function	$-\frac{\left\|x_i - x_j\right\|^2}{2\sigma^2}$

After the selection of kernel function that will be used in SVM module, the SVM module can be implemented. The implemented architecture of SVM module is based classification equation as in Eq. 1 and on the selected kernel function as in Table 1.

According to Eq. 1, RBF can be described as combination of several blocks; each block performs sub function of RBF kernel function. To implement RBF kernel in VHDL it is required to have subtraction, multiplication, and division functions in addition to exponential LUT as seen in Fig. 5 Where SVs are the support vectors that obtained from the training process using MATLAB tool and features are the output of DWT module. To reduce the complexity of exponential function and to save FPGA resources, a LUT is used instead of implementing exponential function. Sigma Parameter (σ) determines the width of well-known bell shape of the RBF. The larger σ the narrower the bell shape of RBF. The value of σ should achieves that the influence region of selected support vectors should include the whole training set.

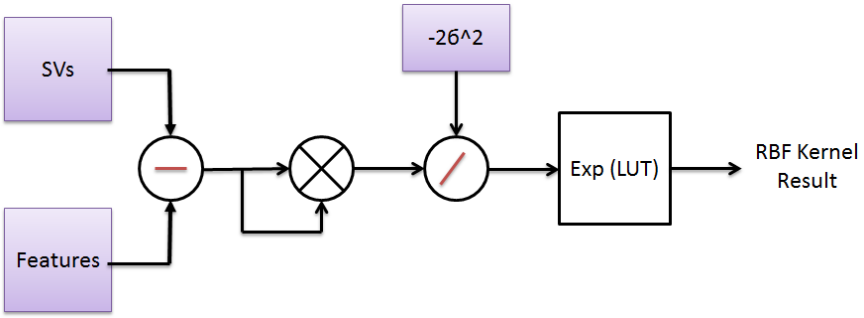

Figure 5 RBF Block Diagram

After implementing RBF function, the classification function (Eq. 1) can be implemented as seen in Fig. 6 where SVM Alphas and bias are obtained during the training process and stored into FPGA design. To get the classification decision, a comparison between the classification function result and zero (0), if the result is greater than 0 the decision is BPSK class and if else the decision is QPSK class.

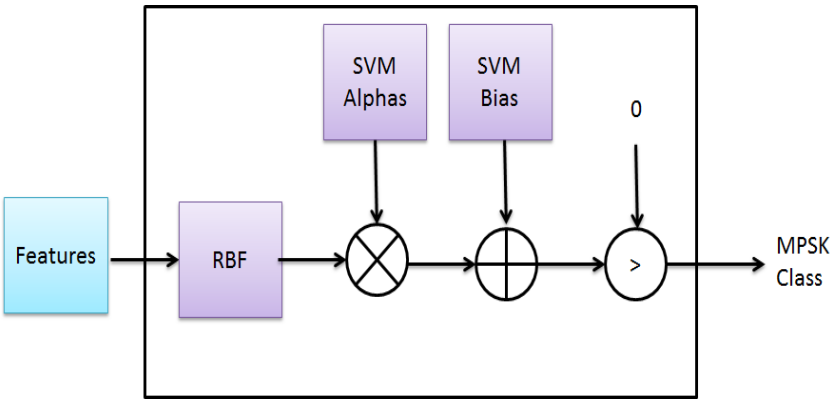

Figure 6 Classification Equation Block Diagram

The SVM module structure consists of subtraction, square, division, multiplication, addition, and comparison processing units. Fixed point functions are implemented in FPGA to perform functions of all the processing units.

Support Vectors (SVs) that are obtained from SVM training data using MATLAB, are stored into Look-up Table (LUT) into FPGA design to be used in the classification process. Features from DWT are subtracted from SVs then the results are squared then divided by $2\sigma^2$ (σ parameter has been selected to be 0.3); next the results are sent to exponential LUT to calculate RBF output. The result from RBF is multiplied by SVM Alpha parameters, which are obtained from SVM training data using MATLAB and stored in Look-up Table (LUT) into FPGA design, then the result is added to the bias constant and the output is compared with a threshold value to classify the received modulated signal as BPSK or QPSK signal as seen in Fig. 7.

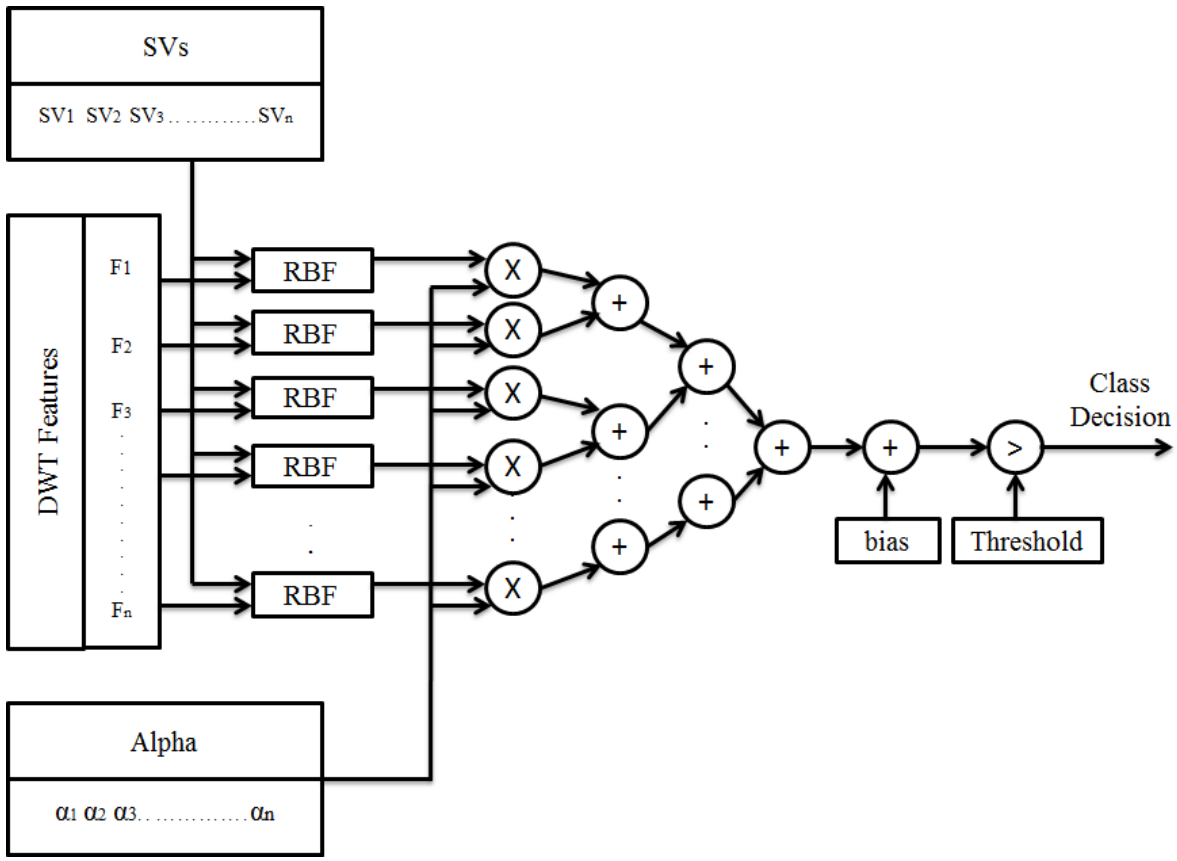

Figure 7 SVM Module Architecture Block Diagram

4. SIMULATION AND RESULTS

Using both Vivado 2015.4 and MATLAB r2015b tools to design SVMC system reduces FPGA power consumption and resources utilization by reducing the complexity of the design. Complex calculation can be performed within MATLAB tool and just the results or some parameters can be used within the designed system on FPGA using VHDL code.

The selection of SVM kernel function is based on the test results obtained from MATLAB r2015b tool by testing different kernel function with the extracted DWT features and comparing the accuracy of them with each other. The comparison result is described as shown in Table 2 and Fig. 8. To perform this test, the features that are extracted from DWT from both BPSK and QPSK are saved into text file during run time using VHDL code. Then MATLAB will load the features file and create a matrix for these features. After that MATLAB have to assign each modulation type to a class. i.e., features that are extracted from BPSK will assign to +1 class and that from QPSK will assign to -1 class. Then these features will be divided into two groups one for train SVM and the other for the testing using svmtrain and svmclassify functions. The results of svmclassify function shows that RBF with sigma parameter of 0.3 has high accuracy than the other functions because it uses radial (nonlinear) separator to solve the optimization problem so it can make boundaries between green circles (QPSK features) and red circles (BPSK features) but the others failed to classify between BPSK and QPSK features because they uses linear separators. According to Table 2 and Fig. 8, RBF is selected to be the kernel function for the SVM.

Table 2 Comparison among Different kernel Functions

Kernel Function	Accuracy (%)
Linear	50.5
Quadratic	61.66
Polynomial	72.70
Radial Base Function	94.44

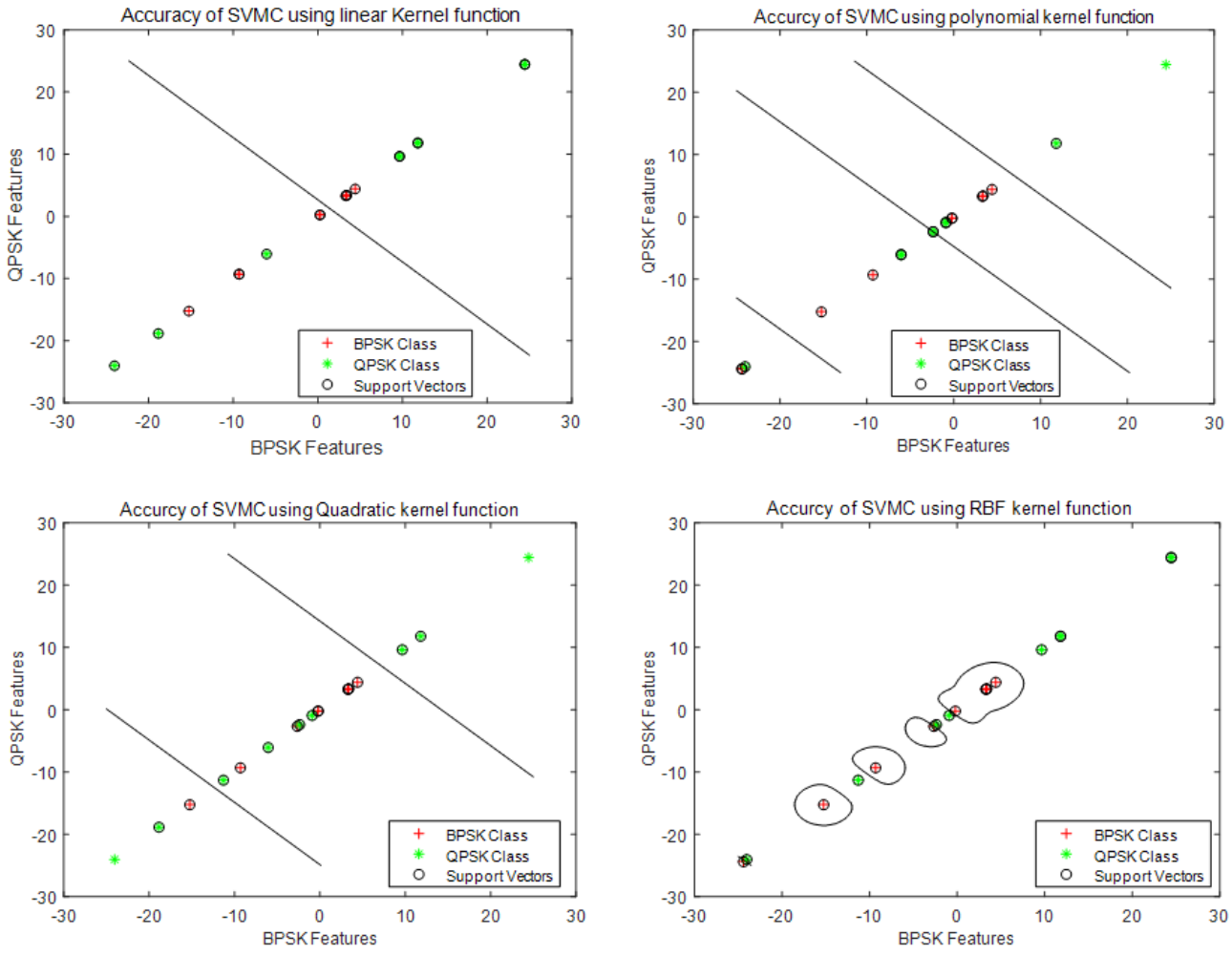

Figure 8 Kernel Functions Comparison Result.

To evaluate SVMC designed system, a Modulation Signal Generator (MSG) module is used. MSG evaluate SVMC by simulating the MPSK (BPSK and QPSK) received modulated signal and this modulated signal is the input to SVMC. MSG consists of phase generator, multiplexer, serial data generator and serial to parallel modules. Phase generator generates four sinewave signals with deferent phases 0, 90, 180, 270, using NCO principle. Based on MPSK selector value (user input switch) one of MPSK modulated signals (BPSK or QPSK) will be generated from the multiplexer. Based on BPSK and QPSK phase selectors values, one of the

phase generator output signals will be selected as an input to the multiplexer. The output from the multiplexer (modulated signal) will be the input to SVMC system as shown in Fig.9. Phase generator generates four sinewaves with different phases 0, 90, 180, and 270 using NCO principle. See Fig.10.

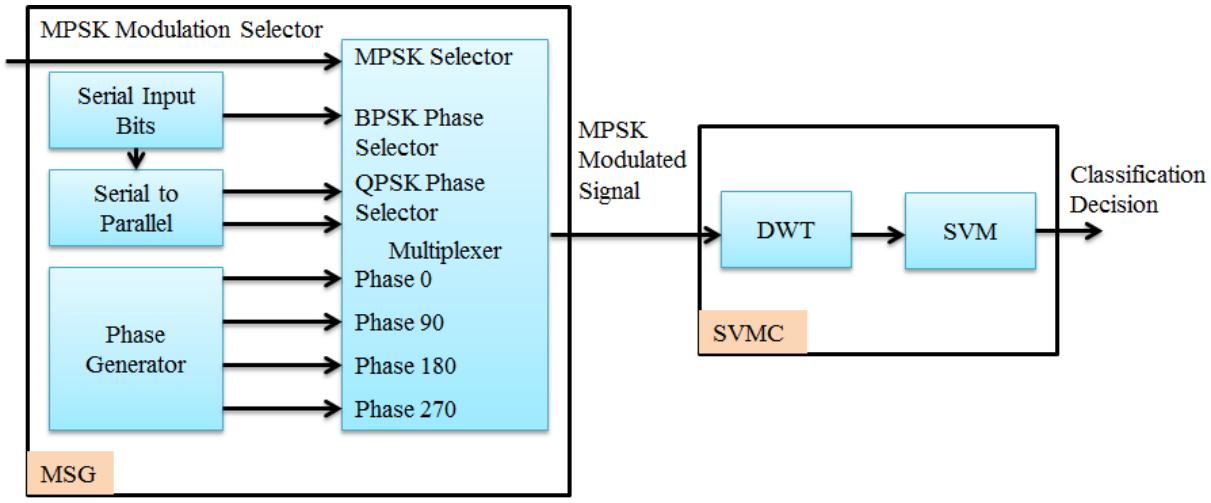

Figure 9 Evaluation and SVMC System Block Diagram

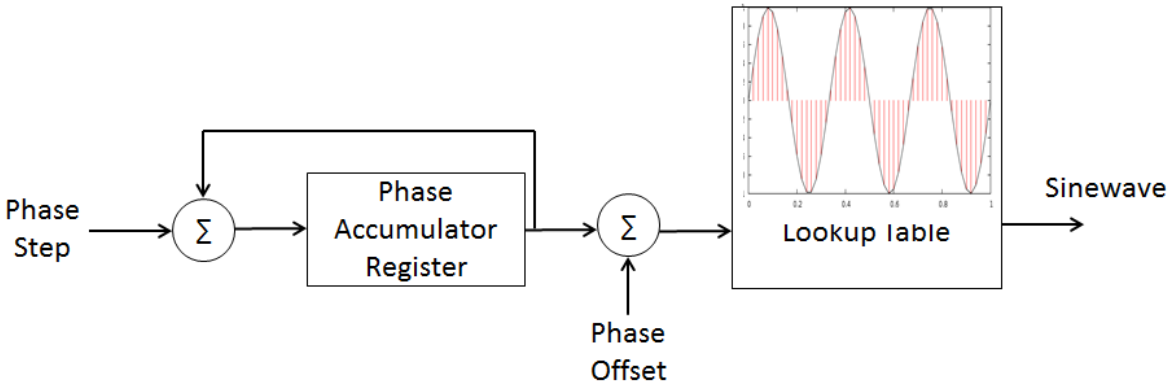

Figure 10 Phase Generator Module Block Diagram

The value of the output frequency (f_{out}) of phase generator determines NCO parameters; phase accumulator capacity, the phase step between each sample of the sinewave samples in LUT, and operating clock frequency. The mathematical representation of NCO module to determine the parameters of phase generation module is in Eq. (2). Based on phase offset value, four sinewaves of different phases 0, 90, 180, and 270 will be generated.

$$f_{out} = \frac{\text{Sinewave Step} \times \text{Clock Frequency}}{\text{Accumulator Capacity}} \tag{2}$$

The simulation result of the implemented classification system using SVM is as seen in Fig. 11.

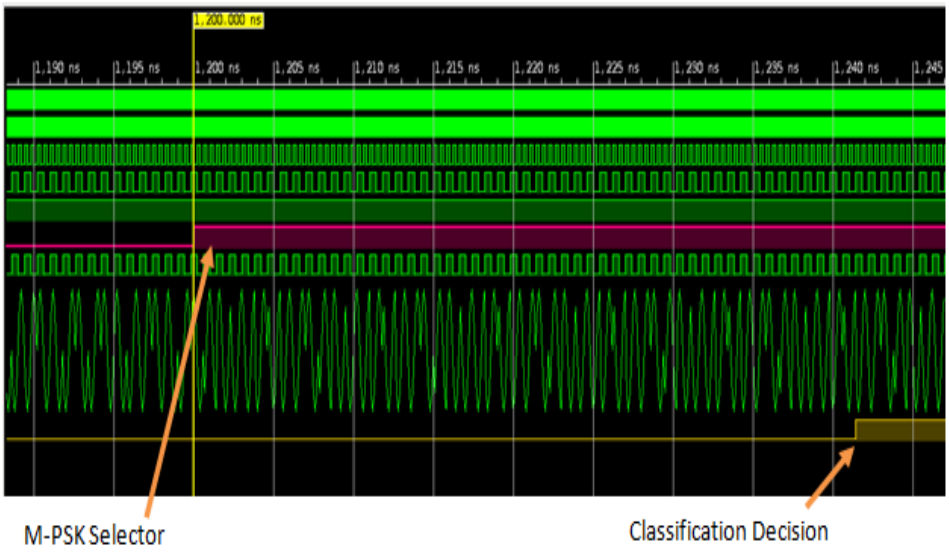

Figure 11 Classification Decision Timing.

The elapsed time from changing the switching key on the board to the classification decision result is about 8.2 ns, and the time that taken by the SVM module to get the classification decision is 2 ns.

For small satellites, it is important to implement the classifier system with less power consumption and resources utilization as shown in Table 3 and Fig. 12.

Table 3: Resources Utilization

Resource	Utilization	Available	Utilization%
FF	1,215	202,800	0.60
LUT	1,309	101,400	1.92
Memory LUT	132	35,000	0.38
I/O	5	285	1.75
DSP 48	42	600	7.00
BUFG	4	32	12.50
MMCM	1	8	12.50

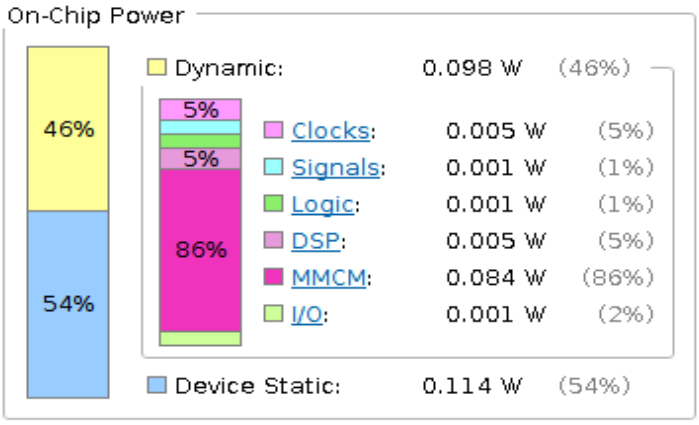

Figure 12: Classifier System Power Consumption.

From Fig. 12, the total power of the whole classifier system is the summation of device static power and dynamic power which is equal 212 mW. So, it can be used for small satellite applications.

Using MATLAB, 100 features of BPSK and QPSK modulations are used to test the performance of AMR system, 4 trials have been applied on 100 features for each modulation technique (for each SNR value) are used to determine the recognition rate of both modulations in the presence of AWGN with SNR from -10 to 20 dB. MATLAB tool can be used to simulate AWGN that can affect received modulated signal at receiver. In that case, MATLAB performs two stages; first stage, MATLAB loads the features file and applying SVM training on the features with the addition of random number. Second stage, MATLAB applies AWGN to modulated data then extracts the features using the same stages and parameters of DWT then applying SVM classification stage then from the result recognition rate can be calculated. Second stage performs in loop to apply different values of SNR from -10 to 20 dB.

The recognition rate can be determined by the following equation Eq. (3).

$$\text{Recognition Rate (RR)} = \frac{\text{Number of correct recognition trials}}{\text{Number of total trials}} \quad (3)$$

The results are compared to previous studied as written in Ref. section to evaluate the performance of the classifier system as shown in Table [4, 5].

Table 4: Comparison between Classifier System and other studies for BPSK

	BPSK						
Studies	-10 dB	-5 dB	0 dB	2 dB	4 dB	8 dB	10 dB
[1]	98.8	99.9	98	-	100		
[2]	98	-	-	-	-	-	100 (at 30 dB)
[3]	-	-	-	91	-	100	100
[4]	-	-	86.3		93	98.2	100 (at 15 dB)
[11]	-	-	98	100	100	100	100
SVMC	98.7	99.8	100	100	100	100	100

Table 5: Comparison between Classifier System and other studies for QPSK

	QPSK						
Studies	-10 dB	-5 dB	0 dB	2 dB	4 dB	8 dB	10 dB
[3]	-	-	-	84	-	96	100 (at 15 dB)
[4]	-	-	85.1	-	92.8	97.3	100 (at 20 dB)
[5]	-	-	1	-	98.5		97.4
[6]	0	-	0	0	47	100 (at 6 dB)	100
[11]	-	-	50	79	80	86	84.5
SVMC	0	1	18	47	70	94.5	100

5. CONCLUSION

Recently, digital modulated signal classification systems are used in military and civilian application. Because of the rabid development of space technology and the increment of cooperation projects in space field, it is required to have GCSs that are capable of recognize all of the modulation techniques and communicate with different satellites (and vice versa) with less complexity and low cost especially it can have a great effect on the future of space communication systems. One of solution is to implement a system that can classify different types of modulation techniques of the received signal which leads to demodulate it by reconfigure a part of FPGA design with the corresponding demodulator using the same configuration without the need for using many Receivers or increase the complexity of the communication system.

For more flexibility in satellite communication system and to overcome communication link problem, one of the solutions is the implementation of SVMC. In this paper, SVMC system is implemented using Vivado 2015.2 and Kintex-7 FPGA kit. SVMC system consists of two modules; DWT module as features extractor, and SVM module as a binary classifier. The evaluation module (MSG) is used to evaluate the performance of SVMC. Two modulation schemes are implemented BPSK and QPSK for simplicity using NCO principle. Many points have to be considered when designing such system as resources utilization, power consumption, classification timing, and recognition rate. From simulation section, the power consumption and resources utilization is considered low and can be used in small satellite application. This system achieves fast classification time about 8.2 ns which is considered fast and suitable for this kind of application, and low resources utilization and power consumption of 212 mW. I.e. the system is suitable even for small satellites. Recognition test has been implemented using MATLAB tool to measure the classification probability under the presence of SNR from -10 to 20 dB. High recognition rate (100%) is obtained for BPSK and QPSK at -6 dB and 10 dB respectively.

6. FUTURE WORK

To improve the capability and performance of SVMC system, several modulation techniques such as 8PSK, 16QAM, MSK, and FSK modulations will be added to the design and SVMC will be improved to be a multi-classes classifier. Also partial reconfiguration technique will be applied on SVMC system to build universal receiver.

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